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Dynamic Range Improvement in Digital to Analog Conversion via Multi-Path Topology

John La Grou[1]

[1] *Millennia Media, SPC, Diamond Springs, California 95619 USA (www.mil-media.com)*

Correspondence should be addressed to Pearl Kohutek (info@mil-media.com)

ABSTRACT

Conventional digital-to-analog conversion (DAC) is accomplished via a single processing path that must optimize broadband noise level against maximum output level, *i.e.,* dynamic range. By splitting DAC processing into two or more discrete elements or "paths," and passively recombining the analog resultants, order of magnitude improvement in dynamic range and linearity can be realized. Following a brief historical review, this paper will explore design details and experimental results on the author's multi-path DAC prototypes, followed by experiments that assess multi-path design margins which exceed required psychoacoustic delivery parameters.

1 Introduction

We define multi-path audio as any capture, creation, transfer, processing, storage, conversion, and/or delivery method employing two or more discrete signal paths or signal elements – with each path, element, process, or method hosting a partial dynamic range (DR) of an original complete audio source or signal.

2 History of Multi-Path Topology

Classic multi-path audio D-A conversion techniques were proposed by JVC Victor Japan in 1981 [1] and NEC Japan [2]. The first DR-improving, multi-path microphone concept may be Analog Devices' *Multiple Microphone* [3], followed by Yamaha and others.

Perhaps the most popular commercial application of multi-path audio is Salzbrenner's *TrueMatch* A-D conversion system, first released in the mid-1990s [4]. As of 2016, Salzbrenner (Germany) is said to have shipped over 100,000 channels of multi-path A-D conversion, placing this among the largest selling high-market A-D converters [5]. Based on recent patent publications (Cirrus Logic, Sound Devices, et al) it is within reason to expect additional DSP-based multi-path commercial activity [6] [7].

3 Multi-Path DAC Topology

Whilst not canonical, for clarity we use the bit convention 1-32, with bit-1 signifying LSB. A 32-bit digital-audio signal represents 192dB of potential DR. We select a target of 26 bits (*i.e.,* bits 7-32) for a usable DR of 156dB, ignoring or discarding incoming "noise bits" 1-6. We assume our program source to exhibit a broadband (20Hz – 20kHz), unweighted noise floor of -140dBu (≈77nVrms) represented at bit 7. This will be our lowest desired program conversion level. This also defines our full-scale level (bit 32) as +16dBu (≈4.9Vrms).

Per Figure 2, our 32-bit PCM audio signal is fed to a 32-bit-capable DSP (*e.g.,* Analog Devices SHARC®, etc.). The DSP is programmed to mathematically adapt the incoming 32-bit signal such that two separate, time-coherent digital output signals are created (*i.e.,* multi-path). The bottom path (Figure 2), what we will call the "low-path," is created from input bits 7 through 25, or 19 bits of audio data, representing the voltage range -140dBu to -26dBu (114dB DR). The upper path, what we will call the "high-path," is created from input bits 26 through 32, or 7 bits of audio data, representing the voltage range -26dBu to +16dBu (42dB DR).

The DSP then sends each path (low-path and high-path) to its corresponding D-A conversion system (DAC IC, buffer, analog filters, I-V conversion, etc.), what we will call the low-path DAC and the high-path DAC, respectively.

4.1 Low-Path DAC

Looking first at low-path processing, the DSP multiplies the low-path signal upward and sends the multiplied signal to its respective low-path D-A conversion. Effectively, the DSP prepends ("pads" or multiplies) the low-path signal with 7 static "null bits" or "dummy bits" [8]. Referring to Figure 1, we see that incoming program bit 7, after DSP multiplication, is delivered to low-path DAC input bit 14. Note that DAC input bit 14 sits at the DAC system's broadband noise floor (-106dBu), thus our low-path DSP multiply assures that all desired low-path information (*i.e.,* input program bit 7 and above) is mapped and retained at or above the low-path DAC systemic noise floor.

But this presents a problem. Input program bit 7, representing a level of -140dBu, is now mapped to a D-A conversion such that the corresponding analog output level will be significantly higher than -140dBu. As seen in Figure 1, our original input program level representing -140dBu, after DSP multiplication, now corresponds to an analog voltage output of -106dBu.

Our low-path DAC IC output is delivering an analog signal that is +34dB higher than the representative digital input signal. We want our original program bit 7 to correspond to a -140dBu analog output, not -106dBu. To achieve our desired low-path analog output level, we now consider a 34dB *attenuation* (-34dB) of our low-path final analog output. This turns our problem into an opportunity.

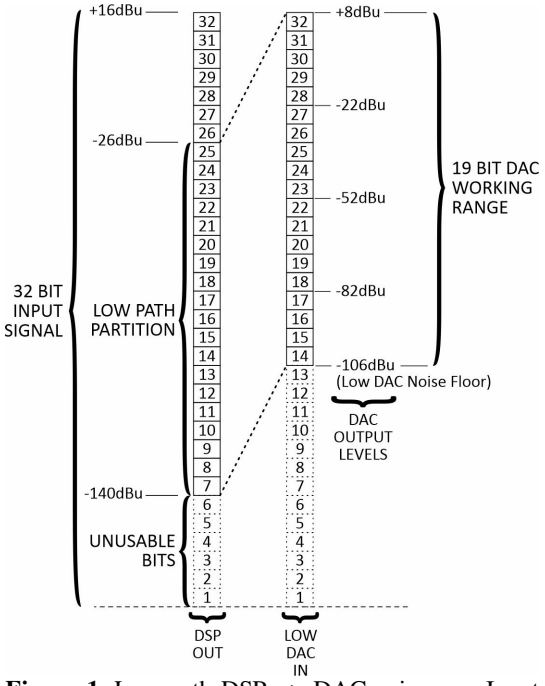


Figure 1. Low-path DSP => DAC gain map. Input signal low-path partition is multiplied by DSP so that incoming LSB (input "bit 7") is shifted into a linear region of the D-A conversion (DAC "bit 14").

Recall (Figure 1) that the broadband, unweighted noise floor of our low-path D-A system is -106dBu (EN_{DAC}). If we place a -34dB attenuator (E_{AT}) following the low-path DAC IC output, we achieve two beneficial results. The first result is that we reduce the low-path partition back to its correctly represented level range (*i.e.,* -140dBu to -26dBu low-path analog range). The second result is that we reduce the low-path noise by 34dB for a resultant low-path output noise of -140dBu plus the broadband thermal noise (EN_{AT}) of the passive attenuator itself. The total low-path noise (EN_{SUM}) is thus given by,

$$EN_{DAC(dBu)} - E_{AT(dB)} + EN_{AT(dBu)} \approx EN_{SUM(dBu)} \quad (1)$$

If the effective resistance of the attenuator (E_{AT}) is low enough, it will add an insignificant amount of thermal noise (EN_{AT}) to the attenuated output (EN_{SUM}) hence achieving our goal of delivering a -140dBu analog signal, or very close to it, at or above the associated low-path analog noise floor.

4.2 High-Path DAC

Now we turn our attention to the remaining top 7 bits (the high-path) with a DR partition represented as -26dBu to +16dBu. In this example, our high-path DAC exhibits -109dBu self-noise with full-scale analog output of +8dBu. From Figure 2, we see that the high-path includes a post-DAC amplifier with +8dB of gain and -109dBu of self-noise, which thus achieves a +16dBu maximum output level with a total path noise of -106dBu, *i.e.,* -109dBu DAC noise added to -109dBu amplifier noise, uncorrelated. When a rising input program signal level reaches very close to -26dBu, the DSP will begin to crossfade the input signal from the low-path to the high-path. The low-path and high-path final analog outputs are passively summed to create a reconstructed single-path analog output signal suitable for line-level use in professional and consumer applications [9].

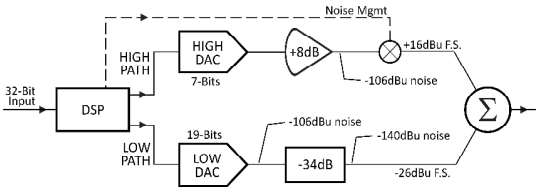


Figure 2. A 26-bit multi-path DAC diagram showing: 32-bit-format PCM digital input signal, DSP processor splitting input program into 19-bit and 7-bit partitions, low-path and high-path D-A conversion elements, low-path attenuator, high-path amplifier, high-path noise management and gate, and passive summing output.

But this presents a problem. The high-path has no attenuation. If we passively sum the low-path output (-140dBu quiescent noise floor) with the high-path output (-106dBu quiescent noise floor), our output noise floor becomes roughly -106dBu. We've lost the benefit of our extraordinary -140dBu low-path noise floor.

4.21 High-Path DAC Noise Control

A solution is found in psychoacoustic theory – and an imperceptible gate. We know that broadband noise is undetectable by the human ear at some point below program signal (*i.e.*, masking). Having found no prior research that looks specifically at perception of broadband noise under mid-level audio program (music, etc.), we targeted a mid-level s/n ratio representative of today's higher-market DAC products, or roughly 80dB (*i.e.,* -26dBu program against -106dBu baseline noise).

We add a DSP-controlled gate or switch point or filter to the high-path analog output after its +8dB amplifier (Figure 2). This signal gate removes the high-path (and its -106dBu noise) from the output summing node. At the point where we close/engage the high-path gate (*nominally* -26dBu), a minimum 80dB program-to-noise ratio is realized.

When a program signal level remains below a defined threshold, DSP prevents (via gate) the high-path from summing with the low-path. With the high-path disengaged from the summing node, only the low-path is connected to the output. Hence, with program levels ranging up to -26dBu nominal, the broadband, unweighted final output self-noise level remains at -140dBu.

When DSP recognizes that the program signal level will rise above -26dBu, the DSP engages the high-path gate, which passively sums low-path and high-path. A brief look-ahead delay processing period is required here, on the order of 1mS. When the low- and high-paths are summed, the output noise floor rises to -106dBu. However, at that moment, our program level has reached -26dBu, which is at least 80dB above the high-path noise floor, making the worst-case transitional (mid-program-level) s/n ratio roughly equivalent to contemporary single-path DAC topologies.

4.3 Dynamic Signal-to-Noise Ratio (DSNR)

A working name is proposed for this mid-level s/n transition: "DSNR" or Dynamic Signal-to-Noise Ratio, *i.e.,* the difference between multi-path signal transition level and output noise level. Minimizing high-path analog noise (combined self-noise of DAC, amplifier-filter, and summing elements) while raising the crossfade level point will correspondingly improve DSNR performance.

4.4 Crossfade Linearity Error (CLE)

A source of DAC multi-path error is encountered during crossfades. Instantaneous level variations are encountered due to gate-state changes and resultant shifts in path impedance bridging (source resistance modulation, or SRM). In blinded lab tests, we find 0.9dB as a worst-case JND (*i.e.,* pure tone) in dynamic path-shift level variation. In design practice, we have achieved an environmentally-stable CLE of 0.03dB – about one-and-one-half orders of magnitude below any perceptible crossfade linearity error.

4.5 DAC Performance

With -140dBu BB/UWTD noise in quiescent and mid-level-program states and ≥80dB below program in high-level-program states, D-A conversion that delivers 26 bits of DR *and* 26 bits of true linearity is achieved. Conventional low-cost DAC IC devices, when combined with novel multi-path processing techniques as described, can achieve DR and linearity of >26 bits, which is an order of magnitude improvement (or more) over today's best single-path D-A topologies. With higher voltage output stages (MOSFET, etc.), >30-bit DAC linearity and DR can be achieved, if desired.

5 Application to Integration

Multi-path conversion systems and processes are well-suited for consolidation into integrated circuits and embedded hybrids. Consider that the main activities of multi-path processing (*i.e.,* DSP, convertors, linear amplifiers, logic and supervisory, resistive attenuation, gating or enabling, summing) can all be integrated onto a single substrate, which would make the scaled IC cost and footprint of multi-path A-D and D-A conversion roughly equivalent to today's single-path IC topologies.

The thoughtful reader will also recognize that multi-path topologies may find far broader industrial uses, such as in audio test equipment (*i.e.,* reduced self-noise), vibrational analysis, high-SPL aerospace testing, medical sensors and instrumentation, seismic testing, and anywhere ultra-wide-DR and ultra-linear processing is required.

6 Conclusion

Beginning with Edison's rollout of acoustic capture and delivery (1880s), the dynamic range of traditional single-path audio has grown historically on a long-average slope of 0.8dB per year. Yet, two-thirds of this 135-year-long audio DR improvement was the result of just three core "paradigm shifts" – (1925) electric capture and delivery, (1950) commercialized magnetic tape, and (1980) A-D / D-A capture and delivery. Each of these three core technology breakthroughs caused an order-of-magnitude (or greater) DR improvement over the previous capture and delivery paradigm [10][11].

Multi-path audio topologies may represent a similar magnitude of improvement, in some applications potentially offering roughly *two* orders of magnitude (100X) DR and linearity improvement over today's best single-path technologies. With integration and miniaturization, multi-path audio processes may ultimately prove practical for transducers / microphones, synthesis, preamplifiers / A-D conversion, DAW processing, D-A conversion, power amplification, and possibly loudspeakers.

Multi-path theory can be applied broadly to both PCM and PDM digital-audio formats; can likely be miniaturized into common ICs; and can be managed using any of today's standard 32-bit-int hardware, networking, and software / file standards.

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Certain design and theory aspects herein are referenced to the author's provisional and published patents: US9,590,648, US9,871,530, US10,256,782, et al.